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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,193	08/18/2003	Azeez Bhavnagarwala	YOR920030289US1 (8728-635	3651

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,193	BHAVNAGARWALA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15-19,26,27,29 and 32-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3-13,15,16,18,19,26,27,29,32-36 and 38* is/are rejected.

7)☐ Claim(s) *17 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 07, 2005, has been entered.

Drawings

3. The drawings are objected to because of the following informalities:

Figures 8 and 9 are objected to because they do not contain descriptive titles. It is suggested that Applicant include titles to the graphs reflecting the information they present, specifically, on page 34, lines 12-17 and page 35, lines 4-9.

As additional clarification, the Examiner suggests that Applicant include a title above Figure 8 stating "Correlations of Measurements of Neighboring Pairs of Transistors" and a title above Figure 9 stating "Distribution Densities of Vt Mismatch".

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any

required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1, 7, and 26 are objected to because of the following informalities:

In claim 1, line 6, to avoid problems of antecedent basis, "semiconductor transistors" should be ---semiconductor transistor devices---.

In claim 1, line 12, to avoid problems of antecedent basis, "semiconductor devices" should be ---semiconductor transistor devices---.

In claim 7, line 2, to avoid problems of antecedent basis, "an integrated circuit" should be ---the integrated circuit--- or ---said integrated circuit---.

In claim 26, line 8, to avoid problems of antecedent basis, "semiconductor transistors" should be ---semiconductor transistor devices---.

In claim 26, line 14, to avoid problems of antecedent basis, "semiconductor devices" should be ---semiconductor transistor devices---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite

for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is considered to be vague and indefinite because it attempts to further limit parent claim 1 by specifying that "the step of obtaining DC voltage characteristic data for the device pair comprises retrieving said DC voltage characteristic data from a database". Parent claim 1, however, specifies "obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage VOUT...wherein VOUT is obtained at a common node connection of the first and second semiconductor transistor devices". It is therefore unclear to one having ordinary skill in the art as to the subject matter which Applicant regards as the invention since it is unclear how a step for obtaining a DC voltage characteristic from a common node connection can be further limited by obtaining the DC voltage characteristic from a database.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 5-10, 12, 26, 27, 29, and 32 are rejected under 35 U.S.C. 103(a) as

being unpatentable over U.S. Patent No. 6,275,094 to Cranford, Jr. et al. in view of Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime".

With respect to claim 1, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

With respect to claims 3 and 29, Cranford, Jr. discloses that the distribution of device mismatch comprises a distribution threshold voltage mismatch (column 7, lines 28-36).

With respect to claims 6, 12, and 32, Cranford, Jr. discloses that the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs (i.e. either p-type pairs or n-type pairs) (column 7, lines 4-9).

With respect to claim 7, Cranford, Jr. discloses determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair (column 1, lines 6-20 and column 4, lines 9-20).

With respect to claim 8, Cranford, Jr. discloses accessing random variation of device mismatch of the semiconductor integrated circuit (column 1, lines 6-20 and column 4, lines 9-20) using variations in the device characteristic for each device of the integrated circuit (i.e. each pair) (column 7, lines 4-9) as determined from distributions of variation of device mismatch for device pairs within the integrated circuit (column 7, lines 20-23 and 28-36).

With respect to claim 9, Cranford, Jr. discloses that the device characteristic comprises threshold voltage (column 7, lines 28-36).

With respect to claim 10, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data (column 7, lines 7-9 and column 8, lines 1-4) for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors (column 7, lines 4-9) in the integrated circuits (column 1, lines 6-20 and column 4, lines 9-20) wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second

transistors (column 7, lines 7-9) and determining a distribution of threshold voltage mismatch for the a selected device pair using corresponding DC voltage characteristic data for the selected device pair (column 7, lines 20-23 and 28-36), determining a threshold variation of transistors in the integrated circuit using one or more determined distributions of threshold voltage mismatch for selected device pairs (column 1, lines 6-10 and column 7, lines 20-23 and 28-36), and characterizing random variations of the integrated circuit using one or more determined threshold variations of transistors of the integrated circuit (column 1, lines 6-20, column 4, lines 9-20 and column 7, lines 20-23 and 28-36).

With respect to claims 26 and 27, Cranford, Jr. discloses implementing the method using a program storage device readable by a machine tangibly embodying a program of instructions (column 7, lines 26-28).

Cranford, Jr. further discloses that the threshold voltage mismatch between the first and second transistors is when the first and second transistors each comprise an NFET (column 7, lines 4-9).

As noted above, the invention of Cranford, Jr. teaches many of the features of the claimed invention and while Cranford, Jr. does teach obtaining DC voltage characteristic of a transistor pair, Cranford, Jr. does not explicitly state that the transistors are operating in a subthreshold region.

Conti teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, "Introduction, lines 1-9 and page 173, column 2, "Mismatch

Model", lines 9-13) by biasing the transistors in a subthreshold region through application of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. to include obtaining the DC voltage characteristic for a transistor pair operating in a subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis and control of mismatch by providing a better estimates of threshold mismatch (page 174, column 1, lines 1-7).

10. Claim 4, as may best be understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti and in view of U.S. Patent No. 6,731,916 to Haruyama.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does obtain DC voltage characteristic data for a pair of transistors, the combination does not specify retrieving this data from a database.

Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to include retrieving the DC voltage characteristic data from a database, as taught by Haruyama, because the invention of Cranford, Jr. and Conti does teach storing the DC voltage data in a look-up table and Haruyama suggests that the combination would have saved time an effort by storing the characteristic data in a database (column 3, lines 14-20 and column 3, lines 42-47) thereby not requiring the process of measuring the characteristic data each time the mismatch is to be determined in the invention of Cranford, Jr. and Conti.

11. Claims 13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 5,999,043 to Zhang et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region, the combination does not explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation.

Zhang teaches an on-chip high resistance device for passive low pass filters with programmable poles comprising a transistor device that is controlled to operate in a subthreshold region through variation in the voltage applied to the gate (column 3, lines 46-49).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region and Zhang suggests a corresponding method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr. and Conti, to obtain accurate threshold voltage mismatch measurements (column 3, lines 46-49).

12. Claims 11 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and Zhang et al. and further in view of U.S. Patent No. 6,819,183 to Zhou et al.

As noted above, Cranford, Jr. in combination with Conti and Zhang teaches many of the features of the claimed invention and while the invention of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed, the combination does not explicitly describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation.

Zhou teaches temperature and process compensation of MOSFETs operating in sub-threshold mode wherein a level of a current source is set to maintain a gate voltage of the MOSFET at a constant below its threshold voltage, thereby maintaining operation in a subthreshold region (column 6, lines 17-21).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr., Conti, and Zhang to explicitly describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed and Zhang suggests another method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr., Conti, and Zhang, when the devices are already operating in a subthreshold region and do not require any variation to obtain accurate threshold voltage mismatch measurements (column 6, lines 17-21).

13. Claims 15, 16, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention, and while the invention of Cranford, Jr. and Conti does teach determining a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table (Cranford, Jr.; column 7, lines 20-23 and 28-36), the combination does not explicitly indicate whether a distribution of input voltages is given for a particular output voltage.

Yoshizawa teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage,

that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of a DC voltage characteristic (column 4, lines 59-67) wherein the threshold voltage can be determined either by determining the distribution of input voltages for a given output voltage or determining a distribution of output voltages for a given input (column 6, lines 6-17).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly include a distribution of input voltages for a particular output voltage, as taught by Yoshizawa, because the invention of Cranford, Jr. and Conti does provide a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table and Yoshizawa suggests a corresponding method for determining such a distribution that would have aided the user by implementing known relationships between input/output voltage and threshold mismatch to allow the user to determine threshold voltage mismatches as part of the look-up table using either known input voltage levels or known output voltage levels as available (column 4, lines 59-67 and column 6, lines 6-17).

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach characterizing mismatch in a semiconductor integrated circuit, the combination does not specify that the integrated circuit be an SRAM.

Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specify that the integrated circuit be an SRAM, as taught by Lovett, because the invention of Cranford, Jr. and Conti does teach employing a threshold voltage mismatch compensated sense amplifier (Cranford, Jr.; column 7, lines 4-5 and 20-23) and Lovett suggests that SRAM devices are devices that employ compensated sense amplifiers (column 1, lines 6-10) and are greatly affected by threshold mismatches due the size constraints of such SRAMs (column 3, line 65 to column 4, line 7) and therefore the combination would have provided greater utility in the invention of Cranford, Jr. and Conti by applying the method to the SRAM devices.

Further, it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136

USPQ 458, 459 (CCPA 1963). In the instant case the structure of Cranford, Jr. and Conti is capable of characterizing transistor mismatch in any of a wide variety of integrated circuits, such as an SRAM, and therefore meets the claim.

15. Claims 19 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 6,798,278 to Ueda.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach a determining a voltage threshold variation of transistors in an integrated circuit using a microprocessor measuring an output voltage as a function of an input voltage, the combination does not specifically indicate determining the variation by determining a standard deviation of threshold voltage variation of the transistors.

Ueda teaches a voltage reference generation circuit and power source incorporating such a circuit wherein a variation in threshold voltage mismatch is determined for a transistor pair by determining a standard deviation (column 13, lines 28-41).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specifically determine a standard deviation of threshold voltage variation of the transistors, as taught by Ueda, because the invention of Cranford, Jr. and Conti does teach determining threshold voltage mismatch indicating the similarity of the transistors using a processor that corrects

for the voltage mismatch and Ueda suggests a corresponding conventional method for determining such variation that would have expressed the variation in terms of a standard deviation that is comparable to accepted limits, thereby increasing the efficiency of the invention of Cranford, Jr. and Conti, by allowing the processor to determine when the variation is outside such limits and the correction needs to be performed (column 13, lines 28-41).

Allowable Subject Matter

16. Claims 17 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because none of the cited prior art teaches or suggests in combination with the other claimed limitations for characterizing device mismatch, determining a distribution of threshold voltage mismatch for the selected device pair using corresponding DC voltage characteristic data, comprising an output DC voltage as a function of an input DC voltage, for the selected device pair by determining a distribution of the input voltage for a given output voltage and determining the distribution of threshold voltage mismatch of the transistors from the distribution of the input voltage corresponding to a distribution of one-half the threshold voltage mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

Response to Arguments

17. Applicant's arguments with respect to claims 1, 3-13, 15-19, 26, 27, 29, and 32-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent Application Publication No. 2004/0193390 to Drennan et al. teaches a method and apparatus for rapid evaluation of component mismatch in integrated circuit performance.

U.S. Patent No. 5,598,115 to Holst teaches a comparator cell for use in a content addressable memory comprising a transistor pair providing a match sense output.

U.S. Patent No. 6,628,146 to Tam teaches a comparator circuit and method that determines a distribution of Vin for Vout of a transistor pair.

U.S. Patent No. 6,161,213 to Lofstrom teaches a system for providing an integrated circuit with a unique identification by plotting a distribution of threshold voltage mismatch between pairs of MOSFETs.

Bastos et al., "Mismatch characterization of small size MOS transistors" teaches a method for characterizing device mismatch in a semiconductor integrated circuit.

Shen et al., "Down Literal Circuit with Neuron-MOS Transistors and Its Applications" teaches a method for determining PMOS and NMOS threshold voltages and corresponding mismatch based on measured Vout vs Vin characteristics.

Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design" teaches the determination of physical causes of mismatch for both p and n-channel devices.

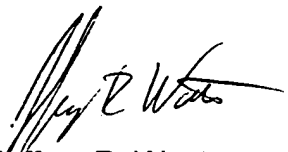
Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems" teaches the determination of subthreshold mismatch in transistor pairs.

Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability" teaches the determination of threshold voltage distribution functions for SRAM devices.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jeffrey R. West
Examiner – AU 2857

January 23, 2006